REMARKS

In the Office Action of December 23, 2005, the Examiner (1) objected to the drawings; (2) objected to the specification; (3) rejected claims 3, 12, and 19 under § 112, second paragraph; (4) rejected claims 1-3, 5-12 and 14-19 as obvious over Feierbach in view of Seal; and (5) rejected claims 4 and 13 as obvious over Feierbach in view of Seal and Jain. In this Response, Applicants amend claims 1, 3, 10, 12 and 19, cancel claims 4, 8-19, 13 and 15-16, and submit new claim 20.

As for the drawing objections, Applicants submit herewith a replacement sheet with a correction to Figures 6 and 7. Further, claims 8-9 and 15-16 have been canceled thereby mooting the claim objection.

Applicants hereby update the list of cross-referenced applications with the serial numbers.

Applicants amend claims 3, 12, and 19 in an attempt to clarify the limitations of those claims. This subject matter is explained in the specification in at least paragraph [0047].

As for the art rejections, claim 1 requires that the "second processor" have a core with "stack storage residing in the core." For this limitation (stack storage in the second processor's core), the Examiner focused on the stack processor 202 and stack 210 of Figure 2 of Feierbach. The stack 210, however, is not shown or described as residing within the core of stack processor 202.

Further, claim 1 requires that and "operating system that executes only on the first processor." Feierbach silent as the existence of an operating system as well as whether an operating system would execute on only one of the processors or on both of the processors. The Examiner argues that Feierbach incorporates Yung by reference. Yung also is silent as to the existence of an operating system. Further, Yung only discloses a single processor and thus does not disclose multiple processors with only one of such processors executing an operating system.

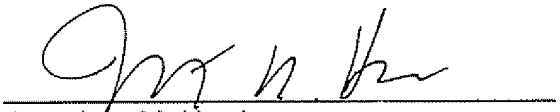
Applicants have amended claim 1 include the limitations of claim 4 but with the "wait" mode replaced with a "reduced power or reduced performance mode." This

limitation is supported at least in paragraph [0006] of the specification. None of the art of record teaches or suggests this added limitation. Claim 20 has been added to depend from claim 1 to further explain that the reduced power or reduced performance mode is one in which a clock internal to the first processor is disabled.

For any or all of these reasons, claim 1 and all claims dependent thereon are allowable. Independent claims 10 and 17, and their dependent claims, are allowable for at least some of the same or similar reasons as for claim 1.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims), Examiner is authorized to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,



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